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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

*U.S. GPO 2000-473-000/44602

Office Action Summary	Application No.	Applicant(s)
	09/405,945	JIN ET AL
	Examiner	Art Unit
	Lynette T. Umez-Eronini	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s)
4) ☐ Interview Summary (PTO-413) Paper No(s).
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue (US 5,378,654) in view of Chang et al. (US 5,893,740).

Hsue teaches in the prior art, a conventional method of forming a self-aligned contact (SAC) on a MOSFET device (column 1, lines 6, 7, 25-27, and Figure 1A-1F). The method comprises forming silicon dioxide **21** (insulating layer) over polysilicon gate structures **15** (transistor gate) and substrate **10** (Figure 1A), forming silicon oxide spacers **18** (insulating sidewalls) on the polysilicon gate structures **15** (Figures 1C-1F), forming a SAC contact opening in the silicon oxide layer **21**, and etching a portion of the silicon dioxide layer **21** that is exposed through a mask **22** to open a portion of the surface of N+ doped region (column 2, lines 14-19). These steps do not include the formation of an etch stop layer over the insulating layer (silicon dioxide **21)**, which reads on, without forming a contact hole etch stop liner.

Hsue differs in failing to teach a transistor have a gate length of less than 0.2 microns, **in claim 1**.

Chang does not teach using the channel field effect transistor in forming a self aligned contact hole, however, Chang uses a gate electrode of 0.1 μm in length to make up a transistor (column 4, lines 55 and 56). Hence, Chang's gate electrode is the same

as a transistor gate and reads on a transistor gate having a gate length less than 0.2 microns.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue by using a transistor with a gate length of less than 0.2 microns as taught by Chang for the purpose of obtaining the claimed invention.

3. Claims 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue (US 5,378,654) in view of Chang et al. (US 5,893,740) as applied to claim 1 above, and further in view of Nulty et al. (US 5,468,342).

Hsue differs in failing to specify processing parameters as recited **in claims 3-11**.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to employ any of a variety of processing variables including those claimed by the applicant. They are well-known variables in the etching art and known to affect both the rate and quality of the etching process. Conducting routine experimentation for the purpose of forming a contact hole would optimize the selection of a particular value.

Hsue in view of Chang differs in failing to teach forming a contact hole includes reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide, **in claims 2 and 3**.

In the art of fabricating semiconductor devices, Nulty teaches forming contact openings in an oxide layer (column 4, lines 21 and 22). The oxide layer be undoped or

doped, for example BPSG (borophosphosilicate glass) (column 1, lines17-25). An opening is formed through the BPSG layer by carrying out the etching in a reactive ion etching system (column 1, lines 14-25 and column 6, lines 15-20 and 54-57, and column 7, lines 4-6 and 17-19). The BPSG layer is deposited by CVD (column 6, lines 12-15), which suggests it is a non-densified doped silicon dioxide layer.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Chang by forming a contact hole that includes reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide as taught by Nulty for the purpose of providing a region whereby contact is made on a semiconductor substrate.

4. Claims 12-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue (US 5,378,654) in view of Chang et al. (US 5,893,740).

Hsue differs in failing to teach etching a first insulating layer comprising doped silicon dioxide, **in claim 12**.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a conventional insulating layer such as silicon dioxide for the purpose of forming a contact region in a semiconductor substrate.

Hsue further differs in failing to teach an etch selectivity between the first insulating layer and the sidewall that is greater than 10:1 and an etch selectivity between the first insulating layer ad the substrate is greater than 100:1, **in claim 12**.

Using the method, oxide insulating layer and insulating sidewall materials of Hsue, which are the same as those of the claimed invention would inherently result in obtaining the same etch selectivities as claimed in the present invention for the purpose of obtaining the best etched product.

5. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsue (US 5,378,654) in view of Chang et al. (US 5,893,740) and further in view of Avinzino et al. (US No. 5,776,834).

Hsue differs in failing to teach

forming a hard mask comprising undoped silicate glass over an insulating layer comprising doped silicon dioxide and the hard mask having openings over a contact hole location, **in claim 17.**

In the art of etching semiconductor material, it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use conventional materials such as undoped silicon dioxide and doped silicon dioxide respectively, as a hard etch mask and first insulating layer for the purpose of forming a contact region in a semiconductor substrate.

Hsue in view of Chang differs in failing to specify a phosphorous doping concentration of greater than 5% by weight, **in claim 19**.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to employ any of a variety of processing variables including those

claimed by the applicant. They are well-known variables in the etching art and known to affect both the rate and quality of the etching process. Conducting routine experimentation for the purpose of forming a contact hole would optimize the selection of a particular value.

Hsue in view of Chang differs in failing to teach forming a contact hole wherein the conducting structures are separated form one another by less than 0.4 microns, **in claims 17 and 18.**

Avanzino teaches a pair of conductive lines having a gap of about 0.5 microns or less (Abstract), which reads on conducting structures that are separated from one another by less than 0.4 microns.

It would have been obvious to one having ordinary skill in the art to modify Hsue in view of Chang by using conductive lines that are less than 0.5 microns or less as taught by Avanzino for the purpose of obtaining the claimed invention.

Response to Arguments

6. Applicant's arguments filed June 14, 2001 have been fully considered but they are not persuasive. Applicant argues the 103 rejection of claim 1 over Hsue and Chang et al. fails to suggest a self-aligned contact hole may be formed without an etch stop liner and may have a transistor gate of 0.2 μm in length and differences in the technologies described in the Hsue and Chang references would fail to make it obvious to combine the references.

Applicant's argument is unpersuasive. Hsue teaches a self-aligned contact that lacks an etch stop (column 1, lines 6, 7, 25-27, and 41-44 and column 2, lines 14-19) but fails to teach a transistor gate having a length of 0.2 μm. Chang is relied upon to teach forming a gate structure having a transistor gate length of less than 0.2 μm (column 4, lines 55). Hsue's and Chang's reference is related to the manufacturing of field effect transistors. Hence, it would have obvious to modify Hsue's gate structure, which is the same as the transistor of the claimed invention, by using a transistor with a gate length of less than 0.2 microns as taught by Chang for the purpose of increasing the speed of the transistor (Chang, column 4, lines 55-64).

Applicant argues the 103 rejection of claims 2-11 over Hsue in view of Chang and further in view of Nulty et al. fails to make it obvious to combine the etch stop liner of Nulty with the no liner method of Hsue and further argues reactive ion etching an insulating layer comprising doped silicon dioxide, where a phosphorous doping concentration is greater than 5 % by weight in claim 3.

Applicant's argument is unpersuasive. Nulty is relied upon to teach a method of forming a contact hole includes reactive plasma etching through a first insulating layer comprising non-densified doped silicon dioxide, which is not taught by Hsue in view of Chang **in claims 2 and 3**.

Nulty teaches forming contact openings in an oxide layer (column 4, lines 21 and 22). The oxide layer may be undoped or doped, for example BPSG (borophosphosilicate glass) (column 1, lines17-25). An opening is formed through the

BPSG layer by carrying out the etching in a reactive ion etching system (column 1, lines 14-25 and column 6, lines 15-20 and 54-57, and column 7, lines 4-6 and 17-19). The BPSG layer is deposited by CVD (column 6, lines 12-15), which suggests it is a non-densified doped silicon dioxide layer.

Hence, it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Hsue in view of Chang by forming a contact hole that includes reactive plasma etching through a first insulating layer comprising a non-densified doped silicon dioxide as taught by Nulty for the purpose of providing a contact region on a semiconductor substrate.

It is noted that Hsue differs in failing to specify a phosphorous doping concentration of greater than 5% by weight, in claim 3.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to employ any of a variety of processing variables including those claimed by the applicant. They are well-known variables in the etching art and known to affect both the rate and quality of the etching process. Conducting routine experimentation for the purpose of forming a contact hole would optimize the selection of a particular value.

Applicant argues the 103 rejection of Hsue in view of Chang for failing to teach the etch selectivity as recited in claim 12.

Applicant's argument is unpersuasive. Hsue differs in failing to teach an etch selectivity between the first insulating layer and the sidewall that is greater than 10:1

and an etch selectivity between the first insulating layer ad the substrate is greater than 100:1, **in claim 12**. However, using the etching method, oxide insulating layer and insulating sidewall materials of Hsue, which are the same as those of the claimed invention would inherently result in obtaining the same etch selectivities as claimed in the present invention for the purpose of obtaining the best etched product.

Applicant argues the 103 rejection of claims 18 and 19 over Hsue in view of Chang and further in view of Avanzino et al. for failing to teach a motivation for combining the references.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, It would have been obvious to one having ordinary skill in the art to modify Hsue in view of Chang by using conductive lines that are less than 0.5 microns or less as taught by Avanzino for the purpose of obtaining the claimed invention.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 703-306-9074. The examiner can normally be reached on First Friday.

FELISA HITESHEW
PRIMARY EXAMINER

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August 15, 2001